CLAIMS

What is claimed is:

1. A method of checking cumulative status of a plurality of arithmetic operations, the method comprising:

initializing a first condition code to a first value;

performing the plurality of arithmetic operations, a result of at least one of the plurality of arithmetic operations being capable of indicating whether a criterion is met;

if the result of at least one of the plurality of arithmetic operations indicates the criterion is met, then initializing the first condition code to a second value;

keeping the first condition code unchanged for a remainder of the plurality of arithmetic operations once the first condition code is initialized to the second value; and

performing a test on the first condition code,

wherein a status of the first condition code indicates a cumulative status of the performed plurality of arithmetic operations.

2. The method of claim 1 wherein the criterion is an item selected from a list comprising the result being non-zero, the result being zero, the result being greater than zero, and the result being less than zero.

3. The method of claim 1 wherein the first condition code is initialized by a non-arithmetic operation.

4. The method of claim 1 wherein the plurality of arithmetic operations are selected from a group comprising a comparison operation and a subtract operation.

5. The method of claim 1 wherein the result of at least one of the plurality of arithmetic operations returns an item selected from a list comprising data equal non-zero, data equal zero, data greater than zero, and data less than zero.

6. The method of claim 1wherein the first value is non-zero.

7. The method of claim 1wherein the second value is a zero.

8. An apparatus to check cumulative status of a plurality of arithmetic operations, the apparatus comprising:

first initializing means to initialize a first condition code to a first value;

processing means to perform the plurality of arithmetic operations, a result of at least one of the plurality of arithmetic operations being capable of indicating whether a criterion is met;

second initializing means to initialize the first condition code to a second value; and

test means to perform a test on the first condition code,

wherein the first condition code remains unchanged for a remainder of the plurality of arithmetic operations once the first condition code is initialized to the second value.

9. The apparatus of claim 8 wherein the first condition code is initialized by a non-arithmetic operation.

10. The apparatus of claim 8 wherein the plurality of arithmetic operations are selected from a group comprising a comparison operation and a subtract operation.

11. The apparatus of claim 8 wherein the first value is non-zero.

12. The apparatus of claim 8 wherein the second value is a zero.

13. A system comprising:

at least one classification engine to classify a selected portion of a plurality of packets; and

an apparatus to check cumulative status of a plurality of arithmetic operations comprising:

a first facility to initialize a first condition code to a first value;

a second facility to perform the plurality of arithmetic operations, a result of at least one of the plurality of arithmetic operations being capable of indicating whether a criterion is met; and

a third facility to initialize the first condition code to a second value if the result of at least one of the plurality of arithmetic operations indicates the criterion is met.

14. The system of claim 13 further including a fourth facility to perform a test on the first condition code.

15. The system of claim 13 wherein once the first condition code is initialized to the second value the first condition code remains unchanged for a remainder of the plurality of arithmetic operations.

16. The system of claim 13 wherein the plurality of arithmetic operations are selected from a group comprising a comparison operation and a subtract operation.

17. The system of claim 13 wherein the first value is non-zero.

18. The system of claim 13 wherein the second value is a zero.

19. The system of claim 13 wherein the classification engine includes a micro-programmed processor.

20. The system of claim 19 wherein the micro-programmed processor selectively processes the selected portion of the plurality of packets by performing thereon at least a subset of packet-based operations including packet header parsing and table lookups.

21. The system of claim 20 wherein the table lookups utilize hash tables.

22. The system of claim 13 wherein a classified packet is returned to the classification engine to be reclassified.

23. The system of claim 13 wherein the classification engine receives a plurality of classification policies to indicate how the classification engine classifies a packet based on select information from a group comprising packet header parsing and table lookups.

24. The system of claim 23 wherein the classification policies are supplied dynamically from an application processor.

25. The system of claim 13 further including an application processor having a host interface.

26. The system of claim 13 further comprising a plurality of data buffers to store data utilized by the system.

27. The system of claim 13 further including an embedded processor to provide processing capabilities to the system.

28. A machine-readable medium that provides instructions which, when executed by a machine, cause the machine to perform operations comprising:

initializing a first condition code to a first value;

performing a plurality of arithmetic operations, a result of at least one of the plurality of arithmetic operations being capable of indicating whether a criterion is met;

if the result of at least one of the plurality of arithmetic operations indicates the criterion is met, then initializing the first condition code to a second value; and

keeping the first condition code unchanged for a remainder of the plurality of arithmetic operations once the first condition code is initialized to the second value.

29. The medium of claim 28 further performing a test on the first condition code.

30. The medium of claim 28 wherein a status of the first condition code indicates a cumulative status of the performed plurality of arithmetic operations.

31. The medium of claim 28 wherein the plurality of arithmetic operations are selected from a group comprising a comparison operation and a subtract operation.

32. The medium of claim 28 wherein the first value is non-zero.

33. The medium of claim 28 wherein the second value is a zero.

34. An apparatus to check cumulative status of a plurality of arithmetic operations comprising:

a first facility to initialize a first condition code to a first value;

a second facility to perform the plurality of arithmetic operations, a result of at least one of the plurality of arithmetic operations being capable of indicating whether a criterion is met;

a third facility to initialize the first condition code to a second value if the result of at least one of the plurality of arithmetic operations indicates the criterion is met; and

a fourth facility to perform a test on the first condition code,

wherein once the first condition code is initialized to the second value the first condition code remains unchanged for a remainder of the plurality of arithmetic operations.

35. The apparatus of claim 34 wherein the plurality of arithmetic operations are selected from a group comprising a comparison operation and a subtract operation.

36. The apparatus of claim 34 wherein the first value is non-zero.

37. The apparatus of claim 34 wherein the second value is a zero.

38. The apparatus of claim 34 further including a micro-programmed processor.

39. The apparatus of claim 34 further including an application processor having a host interface.

40. The apparatus of claim 34 further comprising a plurality of data buffers to store data utilized by the apparatus.

41. The apparatus of claim 34 further including an embedded processor to provide processing capabilities to the apparatus.

42. A method of checking cumulative status of a plurality of arithmetic operations, the method comprising:

initializing a first condition code to a first value;

performing the plurality of arithmetic operations, a result of at least one of the plurality of arithmetic operations being capable of indicating whether a criterion is met;

if the result of at least one of the plurality of arithmetic operations indicates the criterion is met, then initializing the first condition code to a second value; and

performing a test on the first condition code,

wherein a status of the first condition code indicates a cumulative status of the performed plurality of arithmetic operations.

43. The method of claim 42 wherein once the first condition code is initialized to the second value the first condition code remains unchanged for a remainder of the plurality of arithmetic operations.

44. The method of claim 42 wherein the criterion is an item selected from a list comprising the result being non-zero, the result being zero, the result being greater than zero, and the result being less than zero.

45. The method of claim 42 wherein the first condition code is initialized by a non-arithmetic operation.

46. The method of claim 42 wherein the plurality of arithmetic operations are selected from a group comprising a comparison operation and a subtract operation.

47. The method of claim 42 wherein the result of at least one of the plurality of arithmetic operations returns an item selected from a list comprising data equal non-zero, data equal zero, data greater than zero, and data less than zero.

48. The method of claim 42 wherein the first value is non-zero.

49. The method of claim 42 wherein the second value is a zero.

50. An apparatus to check cumulative status of a plurality of arithmetic operations, the apparatus comprising:

a first initializer to initialize a first condition code to a first value;

a processor to perform the plurality of arithmetic operations, a result of at least one of the plurality of arithmetic operations being capable of indicating whether a criterion is met;

a second initializer to initialize the first condition code to a second value; and

a tester to perform a test on the first condition code,

wherein the first condition code remains unchanged for a remainder of the plurality of arithmetic operations once the first condition code is initialized to the second value.

51. The apparatus of claim 50 wherein the first condition code is initialized by a non-arithmetic operation.

52. The apparatus of claim 50 wherein the plurality of arithmetic operations are selected from a group comprising a comparison operation and a subtract operation.

53. The apparatus of claim 50 wherein the first value is non-zero.

54. The apparatus of claim 50 wherein the second value is a zero.

55. An apparatus to check cumulative status of a plurality of arithmetic operations comprising:

a first initializer to initialize a first condition code to a first value;

a first circuit to perform the plurality of arithmetic operations, a result of at least one of the plurality of arithmetic operations being capable of indicating whether a criterion is met;

a second initializer to initialize the first condition code to a second value if the result of at least one of the plurality of arithmetic operations indicates the criterion is met; and

a second circuit to perform a test on the first condition code,

wherein once the first condition code is initialized to the second value the first condition code remains unchanged for a remainder of the plurality of arithmetic operations.

56. The apparatus of claim 55 wherein the plurality of arithmetic operations are selected from a group comprising a comparison operation and a subtract operation.

57. The apparatus of claim 55 wherein the first value is non-zero.

58. The apparatus of claim 55 wherein the second value is a zero.

59. The apparatus of claim 55 further including a micro-programmed processor.

60. The apparatus of claim 59 wherein the first and second circuits utilize the micro-programmed processor to perform their tasks.

61. The apparatus of claim 55 further including an application processor having a host interface.

62. The apparatus of claim 55 further comprising a plurality of data buffers to store data utilized by the apparatus.

63. The apparatus of claim 55 further including an embedded processor to provide processing capabilities to the apparatus.

64. The apparatus of claim 63 wherein the first and second circuits utilize the embedded processor to perform their tasks.